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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,561	08/06/2001	Kazufumi Komura	024016-00012	7046

7590 07/12/2004

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/921,561	KOMURA ET AL.	
	Examin r	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,10,11,18,21-23,26,32 and 35-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,10,11,18,26,35 and 36* is/are allowed.

6)☒ Claim(s) *21-23,32 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 6/14/04 has been entered. Claims 1, 10-11, 18, 21-23, 26, 32 and 35-37 are pending. The amendment and argument overcome the prior art rejections noted in the previous Office action, and therefore, these are withdrawn. In view of a newly discovered prior art, the previous indicated allowable claims 21-23 are withdrawn. New ground of rejections to claims 21-23, 32 and 37 are set forth below. This action is NON-FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 21-22, 32 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,437,618 (Fig. 2), issued to Lee (Lee indicates Fig. 2 is prior art which is known before Jun. 30, 2000).

As per claim 32, Lee discloses a delay circuit (Fig. 2) comprising:

a delay section (210) having two or more delay stages (204 and 205, 206 and 207, ...) connected in series (as shown), each delay stage (for example, 206 and 207) is provided with a serial input terminal (upper input terminal of NAND gate 206) and an individual input terminal (lower input terminal of NAND gate 206) for inputting a signal (the signal received at the lower

input terminal of NAND gate 206), each stage adds a predetermined delay time (this is the delay time of the corresponding delay stage), each delay stage having substantial uniform rise delay time of fall delay time (because each stage has two NAND gates, i.e., even number of NAND gates); and

selecting switch means (201, 202, ...) connected as recited (for example, NAND gate 202 connected to the individual input terminal of NAND gate 206) and receiving an input signal (CLKin) for establishing a delay path from the input signal so that the output signal has a desired delay time (by selecting signals S1, S2, ...), the output signal CLKout has a desired delay time (the recited limitation is merely the result when the selecting signal is selected).

As per claim 21, since NAND gates 206 and 207 functioned as inverters (logic inversion sections) and they are even, the recited limitation is met. Regarding the limitation each inversion section having different propagation delay time between the rise and fall transitions, the recited limitation is met because each NAND gate comprises CMOS transistors which have different rise and fall delay times.

As per claim 22, the recited NAND gates in each stage reads on NAND gates 206 and 207, connected as recited.

As per claim 37, this claim is rejected for the same reasons noted in claim 32.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. US Patent No. 6,437,618 (Fig. 2), issued to Lee.

Lee discloses a delay circuit (Fig. 2) having a structure discussed in claim 21 herein above, he further explicitly discloses each logic inversion section is a NAND gate. Lee does not explicitly disclose each logic inversion section is a NOR gate as called for in the claim.

The examiner takes Official Notice the fact that replacing a NOR gate by a NAND gate to function as an inverter in a delay circuit is old and well known in the art, such teaching can be found in elementary logic circuit textbooks. The concept is so well known that it is a common practice for an assembly worker to replace NAND gates by NOR gates when NOR gates are available or vice versa.

It would have been obvious to one skilled in the art at the time of the invention was made to replace the Lee's NAND gates by NOR gates. The motivation would be save time and money by selecting whatever available when the Lee's delay circuit is implemented.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection and/or the amended claims are allowed.

Allowable Subject Matter

5. Claims 1, 10-11, 18, 26 and 35-36 are allowed. These claims are allowed for the reasons noted in the previous Office action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7/6/04

Minh Nguyen
Primary Examiner
Art Unit 2816